LISTING OF THE CLAIMS:

Claim 1 (Currently Amended) A method of preparing a relaxed SiGe layer on an insulator and a SiGe/Si heterostructure comprising the steps of:

forming a graded $Si_{1-x}Ge_x$ epitaxial layer on a first single crystalline semiconductor substrate,

forming a relaxed $Si_{1-y}Ge_y$ epitaxial layer over said graded $Si_{1-x}Ge_x$ layer,

smoothing the surface of said relaxed $Si_{1-y}Ge_y$ epitaxial layer to provide a surface roughness in the range from about 0.3 nm to about 1 nm root mean square (RMS),

selecting a structure having an upper surface and comprising a second substrate~~, said second substrate with or without an insulator having a major surface with~~ having a surface roughness in the range from about 0.3 nm to about 1 nm RMS and an intermediate agent layer selected from the group consisting of Al, W, Co and Ti, and

bonding said ~~top~~ smoothed surface of said relaxed $Si_{1-y}Ge_y$ epitaxial layer on said first substrate to the ~~top surface of~~ upper surface of said structure including said second substrate, said step of bonding including the step of annealing to form sufficiently strong bonds across the bonding interface to form a single mechanical structure, whereby during said bonding said intermediate agent layer is converted into a metal silicide.

Claim 2 (Withdrawn) The method of claim 1 further including the step of smoothing the upper surface of said relaxed $Si_{1-y}Ge_y$ layer on said second substrate whereby additional epitaxial layers may be grown.

Claim 3 (Withdrawn) The method of claim 2 further including the step of growing an epitaxial layer of a material selected from the group consisting of $Si_{1-y}Ge_y$, Si, SiC, Ge, GeC, and $Si_{1-y}Ge_yC$.

Claim 4 (Withdrawn) The method of claim 3 wherein said $Si_{1-y}Ge_y$ material is selected with a value of y to provide a strained layer or to reduce the bandgap of SiGe to allow absorption of light in the infrared range (>1um in wavelength).

Claim 5 (Withdrawn) The method of claim 1 further including the step of removing said first substrate.

Claim 6 (Currently Amended) The method of claim 1 wherein said ~~low-defect~~ relaxed $Si_{1-y}Ge_y$ layer on said second substrate has a thickness in the range from about 50nm to about 1000nm as determined by the layer structure formed on said first substrate.

Claim 7 (Withdrawn) The method of claim 1 wherein an encapsulation layer of a material selected from the group consisting of Si, SiO_2, Poly Si, and Si_3N_4 is formed on the surface of said relaxed SiGe layer of said first substrate.

Claim 8 (Withdrawn) The method of claim 7 wherein said encapsulation layer is formed and annealed at a temperature in the range from about 400°C to about 900°C.

Claim 9 (Currently Amended) The method of claim 1 wherein said first substrate is selected from the group consisting of Si, SiGe, SiGeC, SiC, GaAs, and ~~or~~ InP.

Claim 10 (Original) The method of claim 1 wherein said step of smoothing further includes the step of Chemical-Mechanical Planarization (CMP) to smooth said surface of said relaxed $Si_{1-y}Ge_y$ layer to provide a surface roughness in the range from about 0.3 nm to about 1 nm RMS.

Claim 11 (Withdrawn) The method of claim 1 wherein after said step of forming a relaxed $Si_{1-y}Ge_y$ epitaxial layer further includes the step of forming an encapsulation layer.

Claim 12 (Withdrawn) The method of claim 11 wherein said step of smoothing further includes the step of Chemical-Mechanical Planarization (CMP) to smooth the surface of said encapsulation layer to provide a surface roughness in the range from about 0.3 nm to about 1 nm RMS.

Claim 13 (Withdrawn) The method of claim 1 wherein an insulator layer is formed on said second substrate for the formation of strained Si/SiGe on insulator and a conducting layer is formed on said second substrate for the formation of p-i-n SiGe/Si heterodiodes.

Claim 14 (Withdrawn) The method of claim 13 wherein said insulator layer includes a material selected from the group consisting of SiO_2, Si_3N_4, Al_2O_3, $LiNbO_3$, low-k materials where k is less than 3.2, or the combination of two or more said materials.

Claim 15 (Withdrawn) The method of claim 13 wherein said conducting layer includes heavily doped p+ Si or p+ Poly Si.

Claim 16 (Withdrawn) The method of claim 13 wherein said insulator layer is formed by a process selected from the group consisting of PECVD, LPCVD, UHVCVD and spin-on techniques.

Claim 17 (Withdrawn) The method of claim 13 wherein said insulator layer is formed at a temperature in the range from about 400°C to about 900°C.

Claim 18 (Original) The method of claim 1 wherein said second substrate is selected from the group consisting of Si, SiGe, SiGeC, SiC, GaAs, InP, sapphire, glass, quartz, $LiNbO_3$, and PLZT.

Claim 19 (Currently Amended) The method of claim 1 wherein said smoothed ~~top~~ surface of said ~~first~~ $Si_{1-y}Ge_y$ relaxed layer on said first substrate is brought into intimate contact with ~~said~~ a top surface of an insulator layer on said second substrate.

Claim 20 (Cancelled)

Claim 21 (Currently Amended) The method of claim 1 wherein said step of annealing includes thermal treatment cycles to form a strong bond at said bonded interface, said thermal treatment selected from the group consisting of furnace anneal, ~~and/or~~ rapid thermal anneal (RTA) and combinations thereof.

Claim 22 (Original) The method of claim 21 wherein said step of annealing includes an anneal ambient selected from the group consisting of air, N_2 and Ar.

Claim 23 (Original) The method of claim 21 wherein said step of annealing includes the step of heating to a temperature in the range from about 100°C to about 800°C.

Claim 24 (Withdrawn) The method of claim 5 wherein a highly selectively wet etching process is used to remove Si substrate of said first substrate.

Claim 25 (Withdrawn) The method of claim 24 wherein EPPW, KOH or TMAH is used as the wet etchant.

Claim 26 (Withdrawn) The method of claim 24 wherein the wet etching in EPPW, KOH or TMAH is at a temperature in the range from about 70°C to about 120°C.

Claim 27 (Withdrawn) The method of claim 24 wherein said step of Chemo-Mechanical Polishing (CMP) includes removing said step-graded $Si_{1-x}Ge_x$ layer and to polish the exposed $Si_{1-y}Ge_y$ relaxed to provide a smoothness in the range from about 0.3nm to about 1nm.

Claim 28 (Withdrawn) The method of claim 24 wherein a relaxed $Si_{1-y}Ge_y$ layer may be epitaxially grown on said top surface of said smoothed relaxed $Si_{1-y}Ge_y$ layer.

Claim 29 (Withdrawn) The method of claim 26 wherein said step of epitaxially growing said relaxed $Si_{1-y}Ge_y$ layer includes growing to a thickness in the range from about 50nm to about 500nm.

Claim 30 (Withdrawn) The method of claim 24 further including the step of growing one of strained Si or strained SiGe or deposition of a n+ Poly Si layer on said smoothed relaxed $Si_{1-y}Ge_y$ layer.

Claim 31 (Withdrawn) A multi layer substrate for use in forming integrated circuits comprising:

a silicon containing substrate,

a silicon oxide layer on said silicon containing substrate, and a relaxed $Si_{1-y}Ge_y$ layer on said silicon oxide layer.

Claim 32 (Withdrawn) The multi layer substrate of claim 31 wherein said silicon oxide layer has a buried upper surface roughness in the range from about 0.3 nm to about 1 nm RMS.

Claim 33 (Withdrawn) The multi layer substrate of claim 31 wherein said relaxed $Si_{1-y}Ge_y$ layer has a buried lower surface roughness in the range from about 0.3 nm to about 1 nm RMS.

Claim 34 (Withdrawn) The multi layer substrate of claim 31 wherein said silicon oxide layer and said relaxed $Si_{1-y}Ge_y$ layer are chemically bonded together.

Claim 35 (Withdrawn) The multilayer substrate of claim 34 wherein said silicon oxide layer bonded to said relaxed $Si_{1-y}Ge_y$ layer has a buried surface roughness in the range from about 0.3 nm to about 1 nm RMS.

Claim 36 (Withdrawn) The multi layer substrate of claim 31 wherein said relaxed $Si_{1-y}Ge_y$ layer has a value y in the range from about 0.2 to about 0.5.

Claim 37 (Withdrawn) The multi layer substrate of claim 31 further including a strained epitaxial silicon containing layer on said relaxed $Si_{1-y}Ge_y$ layer.

Claim 38 (Withdrawn) A multi layer substrate for use in forming integrated circuits comprising:

a silicon substrate, and

a relaxed Si1-yGey layer on said silicon substrate, said relaxed $Si_{1-y}Ge_y$ layer chemically bonded to said silicon substrate.

Claim 39 (Withdrawn) The multi layer substrate of claim 38 wherein said relaxed $Si_{1-y}Ge_y$ layer has a buried lower surface roughness in the range from about 0.3 nm to about 1 nm RMS.

Claim 40 (Withdrawn) The multi layer substrate of claim 38 wherein said silicon substrate bonded to said relaxed $Si_{1-y}Ge_y$ layer has a buried surface roughness in the range from about 0.3 nm to about 1 nm RMS.

Claim 41 (Withdrawn) The multi layer substrate of claim 38 wherein said relaxed $Si_{1-y}Ge_y$ layer has a value y in the range from about 0.2 to about 0.5.

Claim 42 (Withdrawn) The multi layer substrate of claim 38 further including a strained epitaxial silicon containing layer on said relaxed $Si_{1-y}Ge_y$ layer.